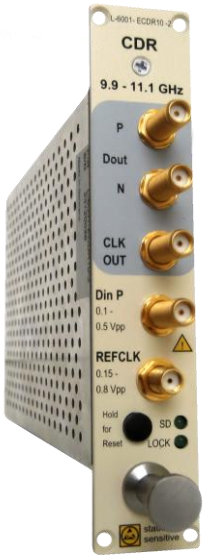
ECDR Module

PN L-6001-ECDR10-2

DESCRIPTION

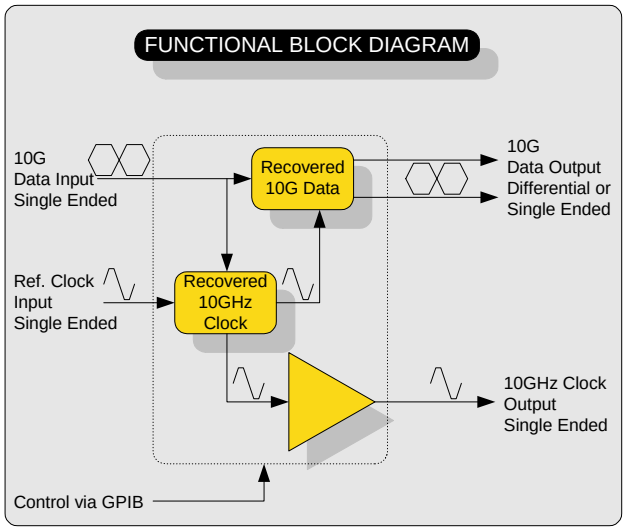
ECDR10-2 is an electrical clock & data recovery module that plugs into the *XBERT* and *ParalleX*™ Chassis. Covering a data-rate of 9.9 to 11.1Gb/s, the module is suitable for applications such as SONET/SDH OC-192/STM64, 10Gbps Fibre-Channel, ITU G.709, and 10Gbps Ethernet. Optionally, operation to 11.3Gbps can be specified. Front panel indicators give immediate status of signal detection and CDR module lock status. Although intended for use with the EBERT pattern generator/error detector, the ECDR10-2 finds a variety of other applications as a low-cost standalone clock & data recovery module.



CLOCK & DATA RECOVERY MODULE PN L-6001-ECDR10-2

KEY FEATURES

- 10GHz range output clock related to data-rate
- 9.9 to 11.1Gbps operation, covering:-
  - OC-192 SONET/STM64 SDH (inc FEC)
  - 10Gbps Fiber Channel
  - ITU G.709
  - 10Gbps Ethernet, IEEE 802.3ae
- Optional operation to 11.3Gbps
- Single-ended data input
- Differential data output with single-ended capability
- Data output polarity swap
- Switchable (on/off) single-ended 10GHz clock output
- LabView™ drivers available
- Small size: width 25.4mm (1”)



XBERT PLATFORM: LETS YOU START SMALL AND GROW BIG

XBERT is a low-cost, modular Bit Error Rate Test Platform used for verification and test of 10Gb/s and above optical and electrical chip, sub assembly and system designs. *ParalleX*™ allows users to perform several BER tests at once using a single clock source. The system is ideal for developers desiring to run simultaneous BER tests on parallel interfaces or multiple independent interfaces. *XBERT* and *ParalleX*™ are scalable so users can start off with a single channel and add modules to grow the system. Manufacturers can realize great savings by taking advantage of the *XBERT* and *ParalleX*™ system’s scalability to perform parallel testing in volume production environments.

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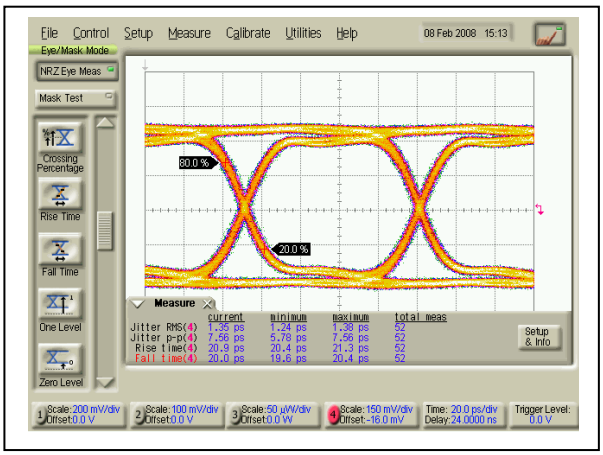
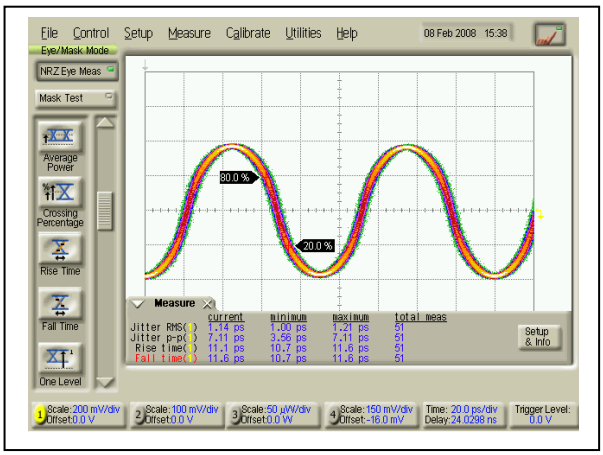
KEY PERFORMANCE PARAMETERS

PARAMETER	SYMBOL	Min	Max	UNIT	NOTE
Data Rate	DR	9.9	11.1	Gbps	Optional 11.3Gbps (opt 103)
Data Input Signal Channel	D_{inP}	100	500	mV_{pp}	Single ended
Data Output Signal Channel	$D_{outP/N}$	575	725	mV_{pp}	Differential Output Voltage
10G Clock Output	CLK_{outP}	700	2100	mV_{pp}	
Reference Clock Input Signal	REFCLK	400	1060	mV_{pp}	
Reference Clock Input Frequency	f_{REFCLK}			GHz	f_{REFCLK} = Data Rate/16
Reference Clock Accuracy		-100	+100	ppm	
Reference Clock Duty Cycle		35	65	%	
Data Output Jitter RMS			1.5	ps	
Data Output Jitter p-p			9	ps	
Data Input Impedance	Z_{inSing}	45	55	Ω	
Reference Clock Input Impedance		45	55	Ω	
Single Ended Output Impedance	Z_{OSing}	45	55	Ω	
Differential Output Impedance	Z_{ODiff}	90	110	Ω	
Operating Temperature	T_{OP}	0	40	°C	Ambient temp.



Data out 11.1 Gbps



Clock out 11.1 Gbps

ECDR10-2

Module

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