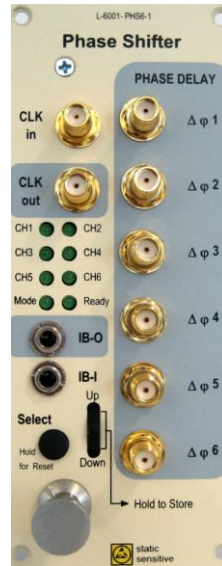


### DESCRIPTION

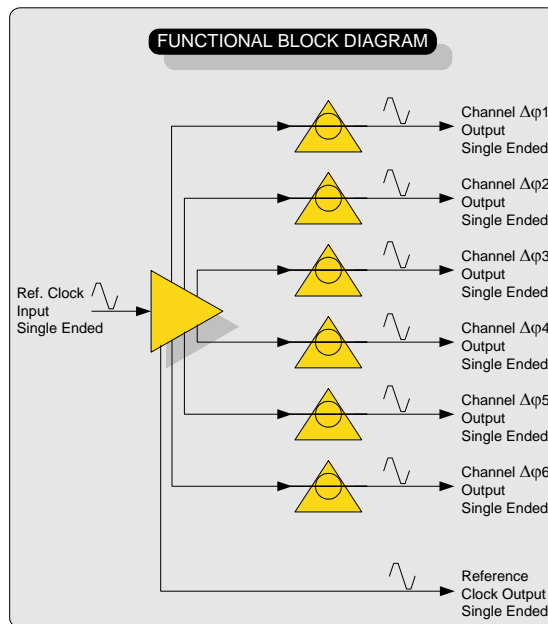
PHS6-1 is a phase shifter module that plugs into the *XBERT* and *ParalleX™* Chassis. The phase shifter module splits the REF-CLK into 6 different REF-CLK output signals, where every REF-CLK output signal can be delayed by up to  $\pm 200$ ps. This allows the user to align the output patterns of multiple E-BERT modules, or to introduce well defined delays. This could help with crosstalk measurements in multi-channel applications for example.



PHASE SHIFTER MODULE PN L-6001-PHS6-1

### KEY FEATURES

- LabView™ drivers available
- GPIB/USB/LAN Interface via XBERT Chassis.
- Small size: width 25.4mm (1")
- Phase shift resolution 1ps with  $\pm 5$ ps accuracy
- Max. phase shift  $\pm 200$ ps with minimum  $\pm 5$ ps and maximum 10% accuracy
- 6 independent phase shiftable reference clock output signals



### XBERT PLATFORM: LETS YOU START SMALL AND GROW



*XBERT* is a low-cost, modular Bit Error Rate Test Platform used for verification and test of 10Gb/s and above optical and electrical chip, sub assembly and system designs. *ParalleX™* allows users to perform several BER tests at once using a single clock source. The system is ideal for developers desiring to run simultaneous BER tests on parallel interfaces or multiple independent interfaces. *XBERT* and *ParalleX™* are scalable so users can start off with a single channel and add modules to grow the system. Manufacturers can realize great savings by taking advantage of the *XBERT* and *ParalleX™* system's scalability to perform parallel testing in volume production environments.

**PHS6-1**  
**Module**  
**Product**  
**Overview**

# Phase Shifter Module PN L-6001-PHS6-1

## KEY PERFORMANCE PARAMETERS

### INPUT

PARAMETER	SYMBOL	MIN	MAX	UNIT	NOTE
Reference Clock Input frequency	$R_{ref}$	400	850	MHz	
Reference Clock Input Voltage Swing	$V_{in}$	500	1400	mV	
Reference Clock Input Termination		AC - coupled			
Reference Clock Input Duty Cycle	$t_{DCin}$	45	55	%	
Reference Clock Input Impedance	$Z_{Ref}$	45	55	$\Omega$	
Reference Clock Rise and Fall time	$t_r / t_f$	90	350	ps	20% - 80%

### OUTPUT DELAYED REFERENCE CLOCK CHANNEL 1-6

PARAMETER	SYMBOL	MIN	MAX	UNIT	NOTE
$\Delta\phi$ Cycle-to-Cycle Jitter	$t_{c-cJ}$		2	$ps_{RMS}$	Note 1
$\Delta\phi$ Total Jitter	$t_{TJ}$		18	$ps_{PP}$	Note 1
$\Delta\phi$ Random Jitter	$t_{RJ}$		2	$ps_{RMS}$	Note 1
$\Delta\phi$ Reference Clock Output Voltage Swing	$V_{out}$	550	950	mV	
$\Delta\phi$ Reference Clock Output Termination		AC - coupled			
$\Delta\phi$ Reference Clock Output Duty Cycle	$t_{DCout}$	40	60	%	
$\Delta\phi$ Reference Clock Output Impedance	$Z_{oRef}$	45	55	$\Omega$	
$\Delta\phi$ Reference Clock Rise and Fall time	$t_r / t_f$	50	350	ps	20% - 80%
$\Delta\phi$ Reference Clock Output phase uncertainty	$R_{PS}$	$\pm 5[ps]$	$\pm 10[%]$		Note 1
$\Delta\phi$ Reference Clock Output phase shift total	$R_{Shift}$		$\pm 200$	ps	$\pm 10%$
$\Delta\phi$ Reference Clock Output increment of phase shift fine tuning	$R_{FT}$		1	ps	Note 2

### MISCELLANEOUS

PARAMETER	SYMBOL	MIN	MAX	UNIT	NOTE
Warm up time	$t_w$	30		min	Note 3
Operating Temperature	$T_{OP}$	10	50	$^{\circ}C$	Ambient temperature

#### Note:

- 1 Depending on stability and quality of input signal.
- 2 Works for a total range of  $\pm 200ps$ .
- 3 Min. warm up time to achieve the specified limits

PHS6-1

Module

Product

Overview



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