**Differential Coder
VWA-28-DIFF-SD**

10 – 28 Gb/s

Description

The **VWA 500023 AA** chip is a NRZ differential coder for high data rate application, typically 10 to 28 (tbc) Gb/s. The chip is designed in 0.18µm SiGe BiCMOS 150 GHz process.

The device has two high frequency differential inputs (NRZ_in and Clock) and one differential high frequency output (DIff_Out). The chip is 50Ω single ended and 100Ω differential in and out. The chip can be used single in and out.

The input data stream is synchronized by the clock and electrically coded to a differential format. If a logical zero is present to the input, the output remains unchanged: Qn+1=Qn. If a logical one is present to the data input, the output value is changed at every rising edge of the clock: a constant one to the input gives a continuous series of 01010 to the output.

The different parts of the chip are internally biased using a voltage and currents reference circuit (Bandgap), in order to have the overall RF characteristics of the chip, insensitive to the voltage supply, the temperature and the process spread. An enable input control pin is used to switch the chip ON or OFF.

Three separate pins are used to bias the chip: one dedicated to the reference circuit, the second for the coder core (input buffers and coder core) and the last for the 50Ω output driver. The 3 bias inputs can be separately filtered / decoupled in order to optimize the overall chip performances.

Applications
- NRZ to RZ DPSK data coding
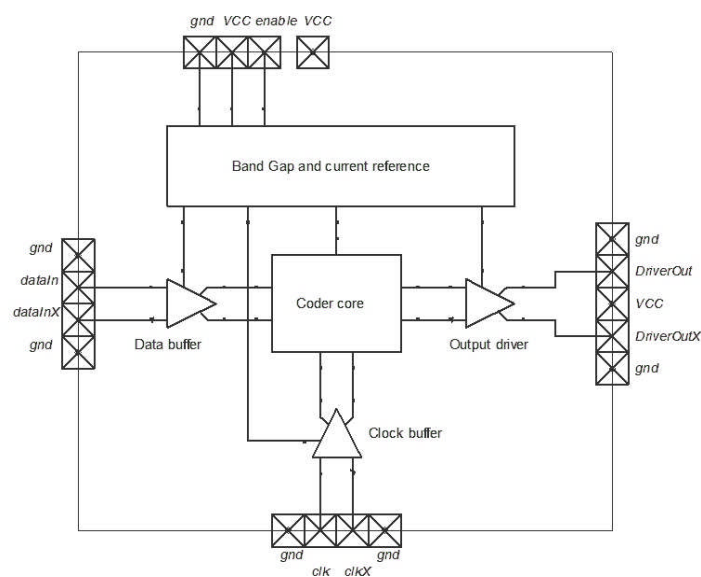- Fiber transmission

Ordering information
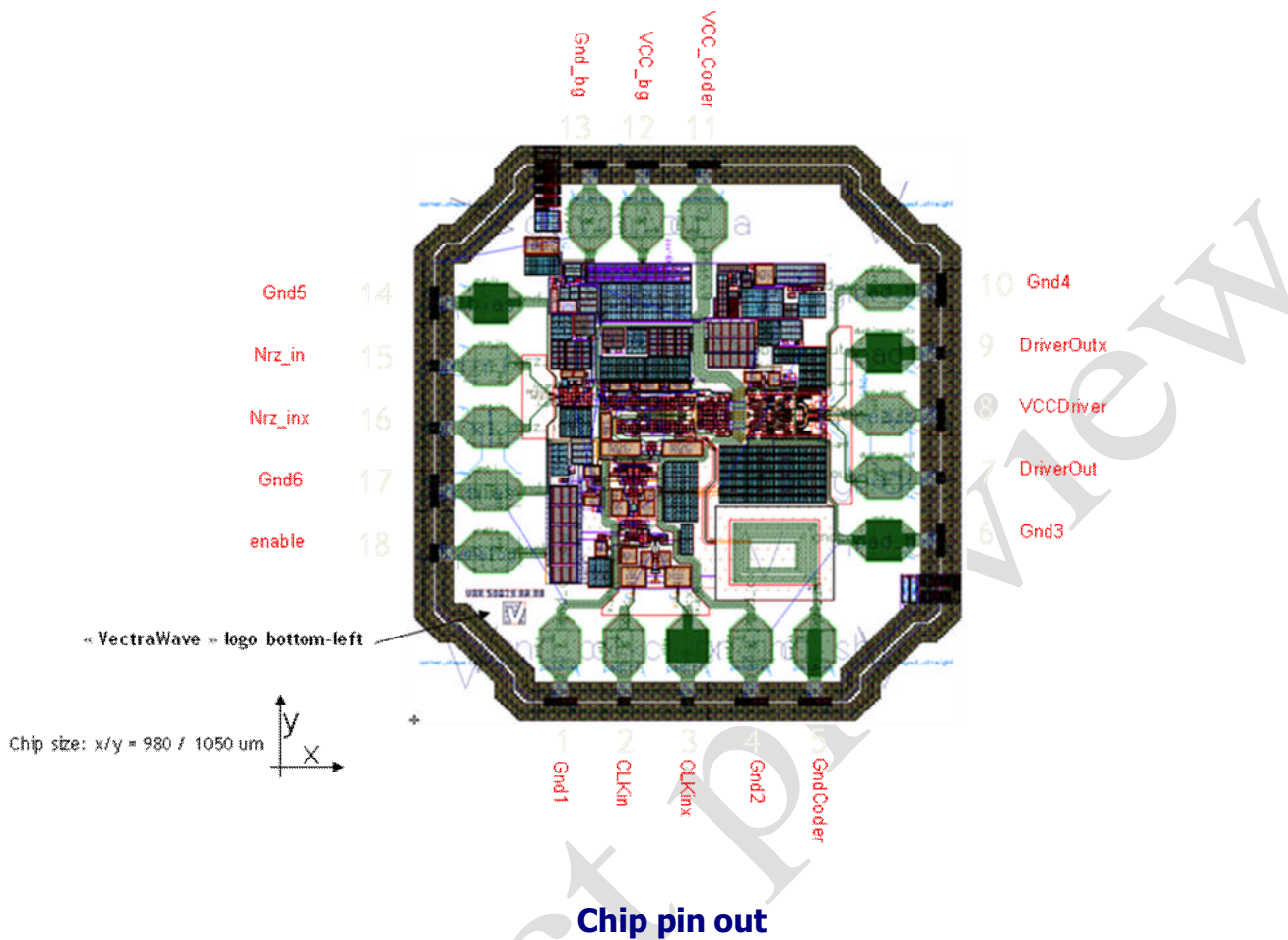**Part Number:** VWA 500023 AA
Demoboard (QFN): VWA 00078 AB

Main Features
- SiGe BiCMOS - Ft = 150GHz
- Data rate up to 28Gb/s
- 3 V / 480 mW typical bias @ 27°C
- Single or differential input / output
- Input amplitude (data and clock): 300mV pp
- Output amplitude: 800mV pp diff (400mV on each 50Ω output)
- Temperature compensated
- ON and OFF state through an enable pin control

Functional Block Diagram

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Gnd_bg VCC_bg VCC_Coder
13 12 11

Gnd5 14
Nrz_in 15
Nrz_inx 16
Gnd6 17
enable 18

10 Gnd4
9 DriverOutx
8 VCCDriver
7 DriverOut
6 Gnd3

« VectraWave » logo bottom-left

Chip size: x/y = 980 / 1050 um

Gnd1 CLKin CLKinx Gnd2 GndCoder
1 2 3 4 5

Chip pin out

Name	Type	Description
Gnd1*	Bias in/out	Ground for clock signal access. To be used with Gnd2 as ground plane for coplanar access.
CLKin	RF input	Clock signal input. **Internally DC decoupled (no external series decoupling capacitor required). Is 100Ω differential with CLKinx**
CLKinx	RF input	Complementary clock signal input. **Internally DC decoupled (no external series decoupling capacitor required). Is 100Ω differential with CLKin.**
Gnd2*	Bias in/out	Ground for clock signal access. To be used with Gnd1 as ground plane for coplanar access.
GndCoder	Bias in/out	Coder core ground access. Is in series with an integrated inductor used to filter the common mode signal due to switching. Can be grounded with an additional external inductor if needed.
Gnd3*	Bias in/out	Ground for signal driver output. To be used with Gnd4 as ground plane for coplanar access.
DriverOut	RF output	RF signal out. The driver uses a 50Ω resistor load in order to be consistent with 50Ω: has to be loaded if not used.

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VCCDriver	Bias in/out	Positive bias for the driver output stage. The DC common output level to the output is directly dependent to this value.
DriverOutx	RF output	Complementary RF signal out. The driver uses a 50Ω resistor load in order to be consistent with 50Ω: has to be loaded if not used.
Gnd4*	Bias in/out	Ground for signal driver output. To be used with Gnd3 as ground plane for coplanar access.
VCC_Coder	Bias in/out	Main chip bias: biases the chip drivers, the coder core and the first driver stages.
VCC_bg	Bias in/out	Chip reference voltage and current bias. Is separated from the main bias to ensure a proper DC filtering
Gnd_bg	Bias in/out	Chip reference voltage and current ground. Is not physically connected to the RF grounds.
Gnd5*	Bias in/out	Ground for input signal access. To be used with Gnd6 as ground plane for coplanar access.
Nrz_in	RF input	Digital signal input. **DC is present on the access. Has to be DC decoupled from the external source by an external capacitor.** Is 100Ω differential referenced to Nrz_inx.
Nrz_inx	RF input	Complementary digital signal input. **DC is present on the access. Has to be DC decoupled from the external source by an external capacitor**. Is 100Ω differential refernced to Nrz_in.
Gnd6*	Bias in/out	Ground for input signal access. To be used with Gnd5 as ground plane for coplanar access.
enable	Digital input	Chip enable: switches the chip ON or OFF.

➢ All pads are octogonal (w / l µm²) = 66 / 105; except VCC_Coder = 75 / 105
➢ Die thickness = 0.28 mm (11 mils)
➢ No metallization on back side

Electrical specifications

Electrical parameters	Conditions	Symbol	Min.	Typ.	Max.	Unit
		Chip bias				
Supply voltage	VccCoder – VccBG	Vcc		3		**V**
	VccDriver		2.5	3	4	**V**
Current consumption OFF mode*	VccCoder; enable=0; T=27°C	VccCoder0		3		**nA**
	VccBG; enable=0; T=27°C	VccBG0	(100°C) 0.01	15	(-40°C) 28	**uA**
	VccDriver; enable=0; T=27°C	VccDriver0		27		**pA**
Current consumption ON mode*	VccCoder; enable=1	VccCoder1		20		**mA**
	VccBG; enable=1	VccBG1	(-40°C) 2		(100°C) 2.5	**mA**
	VccDriver; enable=1	VccDriver1		150		**mA**
		Data input (Nrz_in and Nrz_inx)				
Input impedance	Single and differential modes	Zin		100		**Ω**
Amplitude range**	Single or differential input		2	300		**mVpp**
		Clock input (Clkin and Clkinx)				
Input impedance	Single and differential modes			100		**Ω**
Amplitude range**	Single or differential input		1	300		**mVpp**
Frequency range***					25	**GHz**
Phase margin				Tbit/4		
		Driver Output				
Output impedance	Single / Differential			50 / 100		**Ω**

Common mode voltage	Referred to VCCDriver			VCCDriver-0.350		**V**	
Amplitude	Single			400		**mVpp**	

* OFF → enable ="0", ON → enable="1"
** The Min value corresponds to the sensitivity.
*** The frequency range is given in GHz for the clock signal. It corresponds to the data rate.
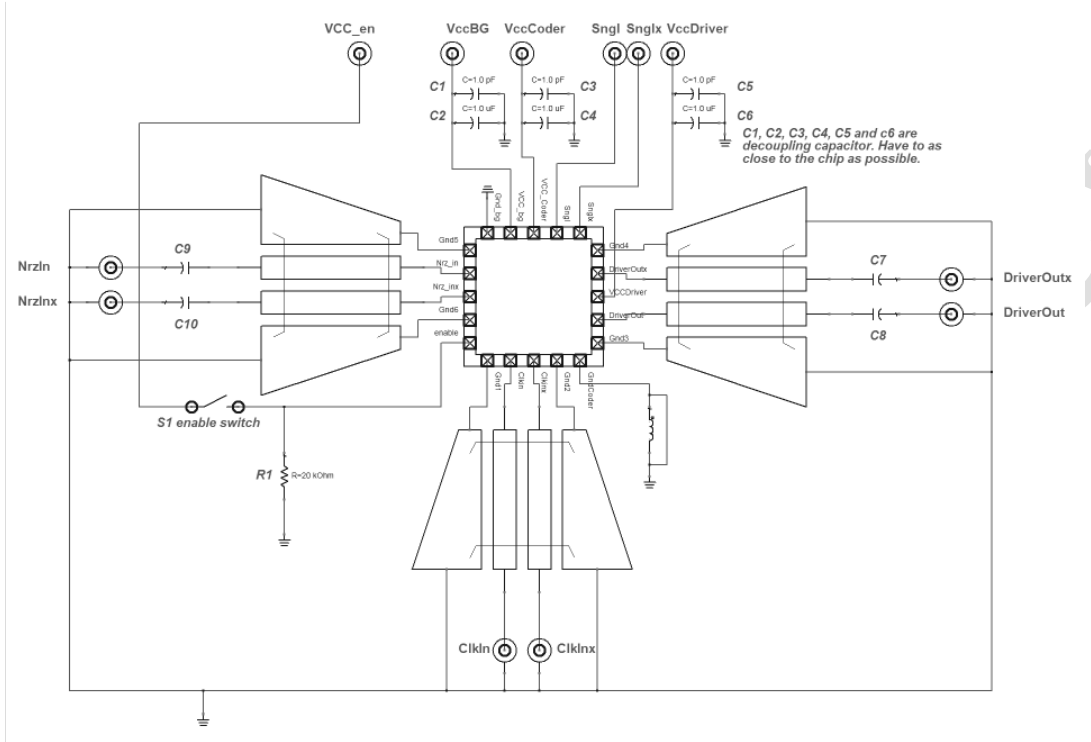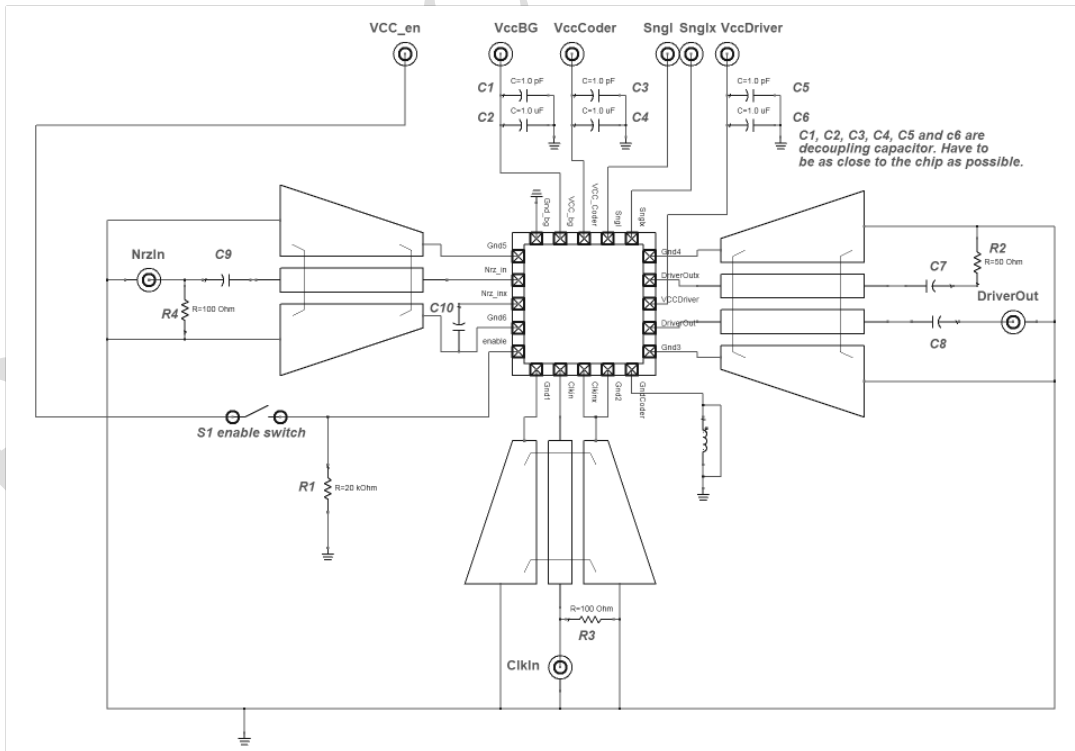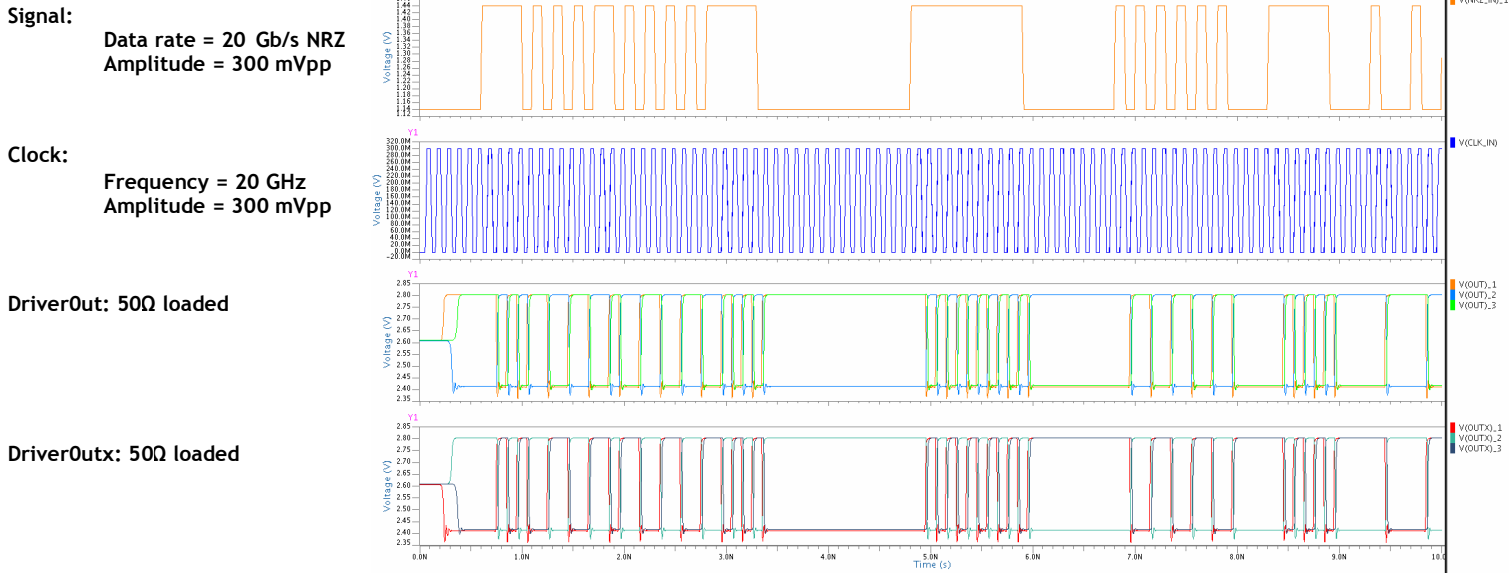
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Absolute rating

Parameters	Conditions	Symbol	Min.	Typ.	Max.	Unit
Supply voltage	VccCoder – VccBG - VccDriver	Vcc	-0.5		4.6	**V**
Digital input	enable		-0.5		4.6	**V**
Storage temperature					TBC	**°C**

ESD protection

Parameters	Conditions	Symbol	Min.	Typ.	Max.	Unit
HBM* rating RF in/out	Clk, NRZin DriverOut				0.9	**kV**
HBM* rating analog	enable				2.3	**kV**
HBM* rating bias	VCC gnd				5.7	**kV**

*Human Body Model

Application schematic

Differential IN and OUT

Single-ended IN and OUT

Output characteristics – simulated

Typical coder response: for -40 (_1), 27 (_2) and 100 (_3)°C - RC parasitics

Signal:
> Data rate = 20 Gb/s NRZ
> Amplitude = 300 mVpp

Clock:
> Frequency = 20 GHz
> Amplitude = 300 mVpp

Driver0ut: 50Ω loaded

Driver0utx: 50Ω loaded

Handling

These products are sensitive to electrostatic discharge and should not be handled except at a static free workstation. Take precautions to prevent ESD; use wrist straps, grounded work surfaces and recognized anti-static techniques when handling the IC.

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