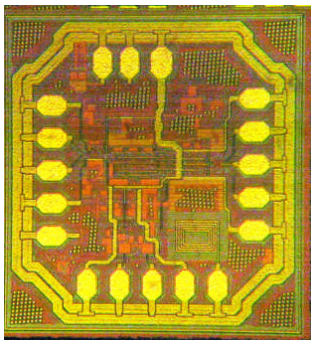


VWA-50011 AA

Power Controller for high data rate application

Description

The **VWA-50011 AA** is a power controller for high data rate application. it is used into the TX modules that are used to drive the data to the MZ $LiNbO_3$ optical modulator. This type of device requires a drive voltage of about 8 to 10V typically that has to be continuously monitored and controlled. *The controller has been developed with the Jazz SBC18 process, using its high speed HBT option in order to integrate the detector on chip. Therefore, the chip can directly be used into a module as GaAs PA companion with no additional diode detector.*

For this type of application, the PA or data driver is generally a GaAs distributed amplifier 100 KHz to 15 GHz for a 10 Gbits/s application. Its output level is coupled to the detector input in order to ensure a level of about 1 Vpp. The controller input stage is a peak detector, linear in linear (means that the detector output level is proportional to the amplitude of the signal and not to the power in dBm).

The power control principle consists in comparing the detected power value to an external wanted (set) value; the control loop modifies the PA gain / power control DC voltage value in order to match the wanted value to the set value. If a voltage ramp is applied to the set value, the PA output amplitude increases linearly.

The specification is closely linked to the high data rate application, where there is no need for a high control dynamic range, but for an accurate output level control. *The detector is very application-specific: this is truly the part that has to be redesigned accordingly to the frequency, the dynamic and the process. The main part, which is the controller core, has been designed in CMOS. It is a design platform which is used into our controller family. The specifications can be modified upon customer's requests.*

Features

- Temperature and process compensated
- Dynamic range: linear from 0.2 to 1 Vp (no damage): single ended input.
- 2.9 to 3.3V voltage supply.
- Setting value from 0.3 to 1.8V full scale.
- External 50Ω resistor to the match the detector input
- External capacitor for feedback loop stabilization.

Advantages

The level control using the VWA 50011 AA does not have to be at "system level" as it is classically done.

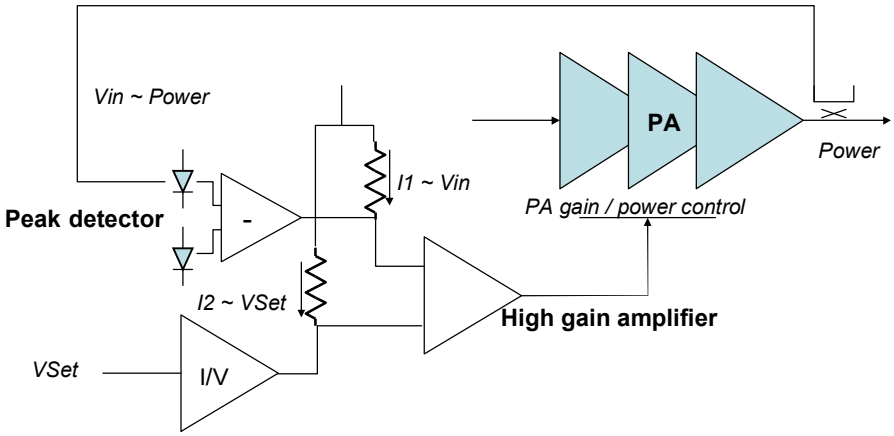
The controller includes a peak detector which is internally compensated (temperature and process). The output level is only linked to the Set Value, applied to the controller, independently of (Output-Level) VS (Gain / Level-Control) driver characteristics.

The driver characteristics dispersion (process) and variation (temperature and aging) are compensated by the control loop. A calibration at system level is no longer required.

Applications

- OC192-STM64-10GE long haul transmission
- SONNET –SDH optical systems
- Single MZ modulator solutions
- RZ DPSK coding

Simplified Functional Block Diagram



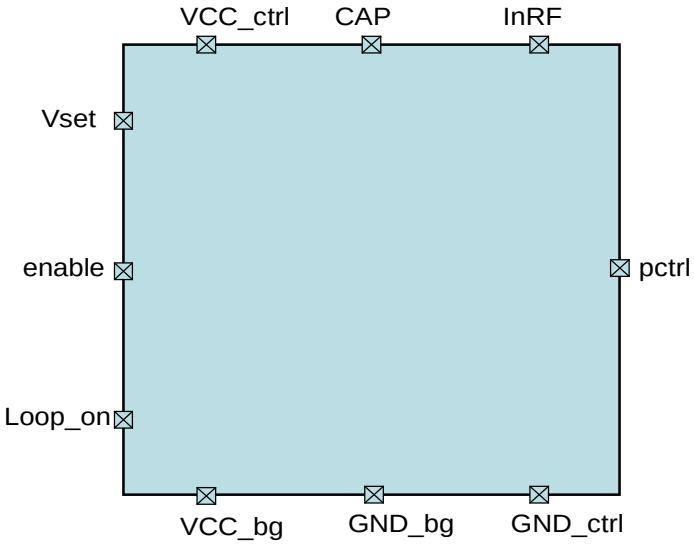
A part of the signal to the driver (PA) output is coupled to the peak detector. It uses two equivalent devices, one being used as reference. The actual signal level is the difference between the detected signal and the reference. The detected signal level is compared to the wanted value VSet and a High gain amplifier is used to close the loop. The signal to the High gain amplifier output, which control the driver level, is such that Vin ~VSet.

A scalling and offset can be done thanks to the use of the gm (I/V) device, loaded by a resistor depending on specific needs t is possible to have Vin (Driver Output Level) = α x VSet + β.
For the WVA 50011 AA, α ~ 2, β = 0

Pad list and description

Pad number	Pad Name	Description
1	VCC_bg	POWER supply for the internal voltage / current reference generator.
2	Gnd_bg	Voltage / current generator GROUND
3	Gnd_ctrl	Main controller (including the detector) ground
4	pctrl	ANALOG output: sets the PA gain level according the setting level (vset)
5	InRF	RF detector input
6	CAP	ANALOG input / output: stabilization capacitor
7	VCC_ctrl	POWER supply for the main controller part
8	vset	ANALOG input. Driver level setting value
9	enable	DIGITAL: set the chip ON = 1 / OFF = 0
10	Loop_on	DIGITAL: opens the loop = 0 / closes the loop = 1 If Loop_on = 0, pctrl stays unchanged independently to vset and InRF.

Chip pad-out



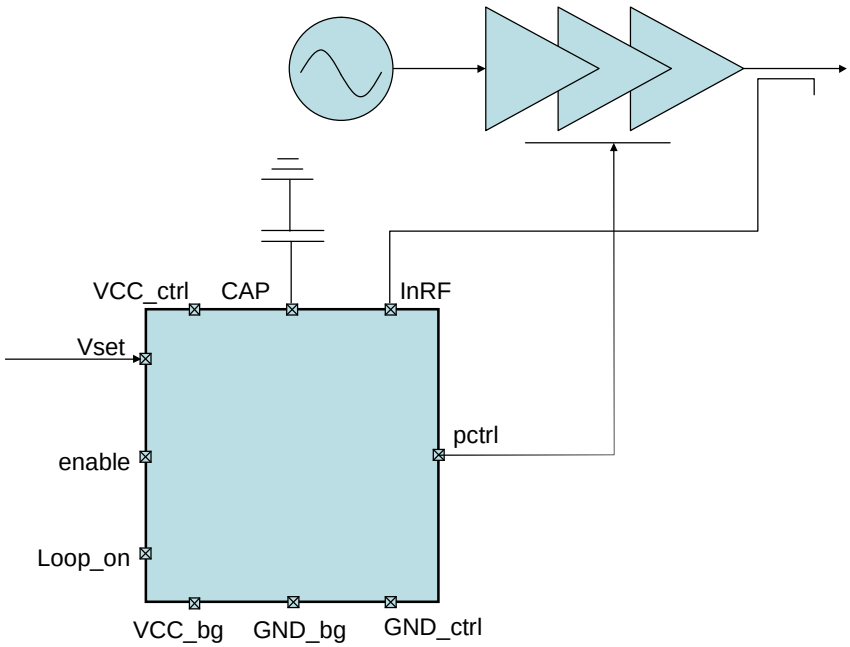
Measurement setup:

Nominal operation

For a nominal operation condition with a given VSET, the control loop is:

- **InRF** – peak detector – high gain stage – gain control buffer – **pctrl**

The PA output is coupled to the controller input **InRF**. The signal to InRF input has to be in the 0.2 to 1Vp range. The PA output level is controlled by the pad **pctrl** connected to the PA gain / power control pin. An external capacitor (typically uF) has to be connected to **CAP** to stabilize the loop. The value required depends on the PA (Pout VS gain control) transfer function.



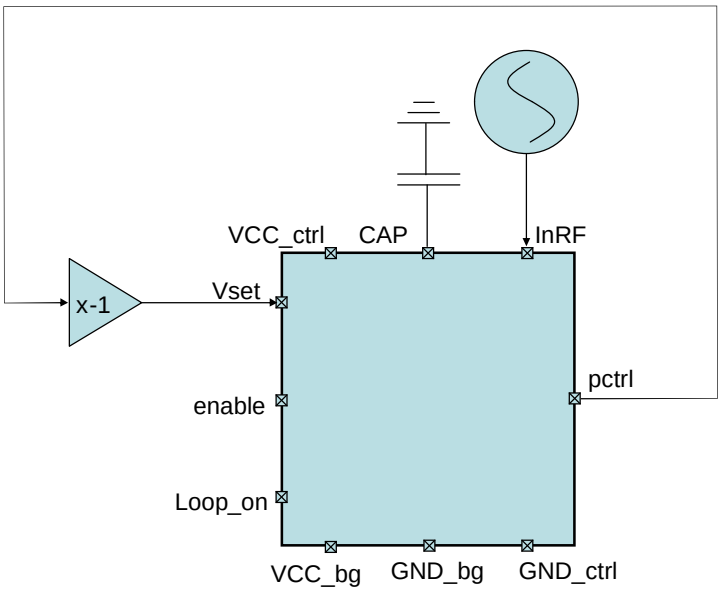
Power control characterization

The setup used to characterize the controller itself is slightly different to the previous one. The power source is directly applied to the controller RF input (InRF) and then the control loop is:

- Vset – gm amplifier - high gain stage – gain control buffer – **pctrl – (x-1)**

An external inverter is required (x-1) to add 180° phase into the loop and ensure the stability. As the loop is not designed to be used this way, additional decoupling capacitors may be required as well.

In the test condition reference PA is no longer required



Overall Specification

Parameter	Conditions	Min	Typ	Max	Units
Power supply: VCC_ctrl and VCC_bg					
Supply Voltage	VCC	2.9		3.3	V
Supply Current*	Enable High		6	10	mA
Shutdown Supply Current	Enable Low			1	uA
InRF pad: detector input					
Frequency Range (peak detector)				30	GHz
RF input voltage range (linear range)		0.2		1	Vpp
Slope (VSet / VRF pp)	RF freq=10 GHz		1.8		
Intercept	RF freq=10 GHz		0		V
RF Input Resistance**			2		kOhm
RF Input Capacitance**			1		pF
Digital inputs: enable and Loop_on					
Logic Low				0.8	V
Logic High		1.8			V
VSET pad: setting value					
VSet Input Range		0.4		1.8	V
VSet slew rate			16		V/us
VSet Input Resistance (CMOS gate)		30			MOhm
pctrl pad: PA power control					
Output Voltage Range (PA power control)	Pctrl pin	0.2		VCC_ctrl – 0.2	V
Output Current			14		mA
Output Slew Rate	No Capacitor on Filter		20		V/uS
Output Buffer Noise			25		nV/√Hz
Die Size	TBC			0.980	mm^2

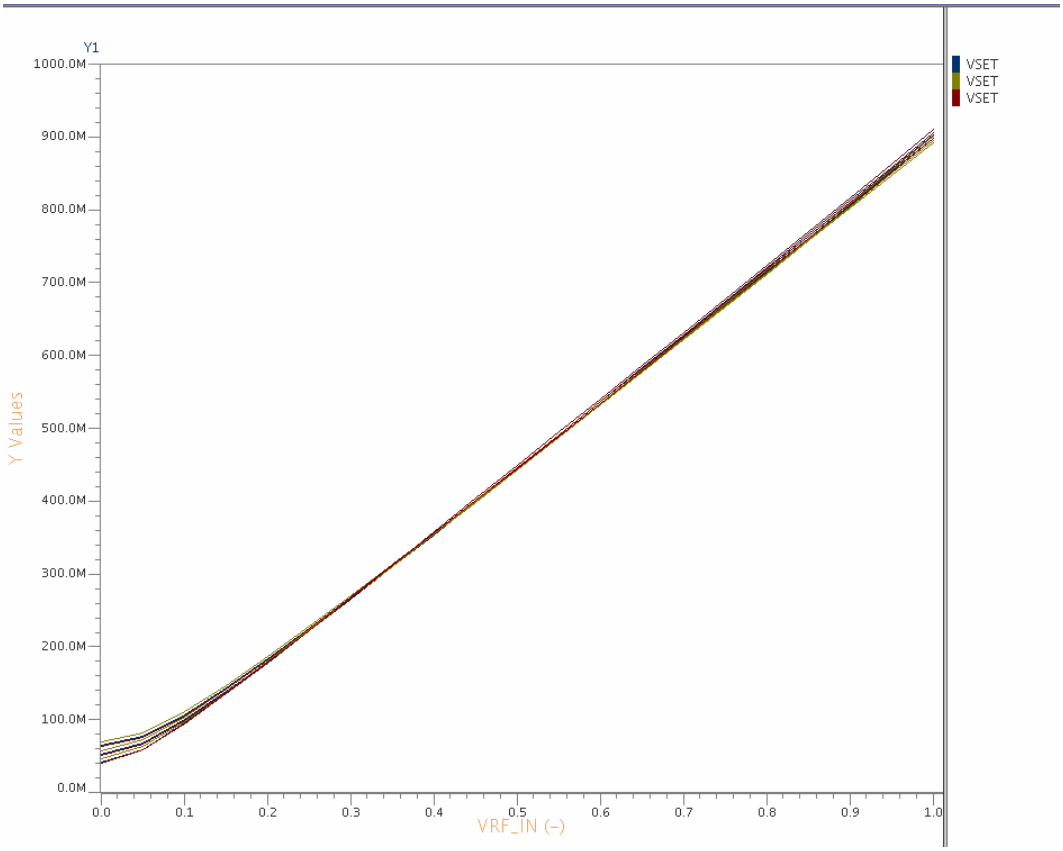
** Not including the current control to the PA*

*** The 50Ω matching is made with an external resistor*

On Chip Characteristics:

The following characteristics have been simulated using the "power control characterization" setup as previously described. The power source is directly connected to the detector input and the loop is closed between pctrl and VSET

The simulations have been made over process for -40, 27 and 100°C



Environment Parameters

Maximum ratings	Symbols	Min	Typ	Max	Units
Operating temperature (case)	Top	-40		+100	°C

Handling

This product is sensitive to electrostatic discharge and should not be handled except at a static free workstation. Take precautions to prevent ESD; use wrist straps, grounded work surfaces and recognized anti-static techniques when handling the **VWA-50011 AA** chip.

Care should be taken to avoid supply transient and over voltage. Over voltage above the maximum specified in absolute maximum rating section may cause permanent damage to the device.