

Differential Amplifier VWA-40-DIA-SD
DC – 40 Gb/s

Description

The **VWA 50030 AA** chip is a limiting - high gain differential amplifier for high data rate application, typically 10 to 40 Gb/s. The chip is designed in 0.18µm SiGe BiCMOS 150 GHz process.

The chip can be used in various ways:

- Single ended input to differential output transformer, by grounding through a capacitor one of the inputs.
- Limiting amplifier, using the high linear gain to saturate the input signal.
- Cross point control which can be done by adjusting the DC levels between the two inputs.

The amplifier is a 6 stages amplifier, giving typically 60dB linear gain. When in saturation, the output amplitude is 400 mV pp single ended (800 mV differential pp).

The different parts of the chip are internally biased using a voltage and currents reference circuit (Bandgap), in order to have the overall RF characteristics of the chip (especially the output amplitude), insensitive to the voltage supply, the temperature and the process spread. An enable input control pin is used to switch the chip ON or OFF.

Three separate pins are used to bias the chip: one dedicated to the reference circuit, the second for the amplifier core (input buffers and amplifier core) and the last for the 50Ω output driver. The 3 bias inputs can be separately filtered / decoupled in order to optimize the overall chip performances.

Applications

- Limiter.
- Single to differential transformation.
- Cross point control.

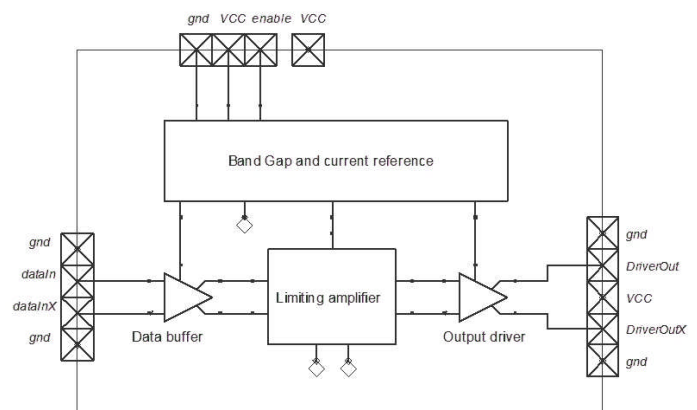
Ordering information

Part Number: VWA 50030 AA

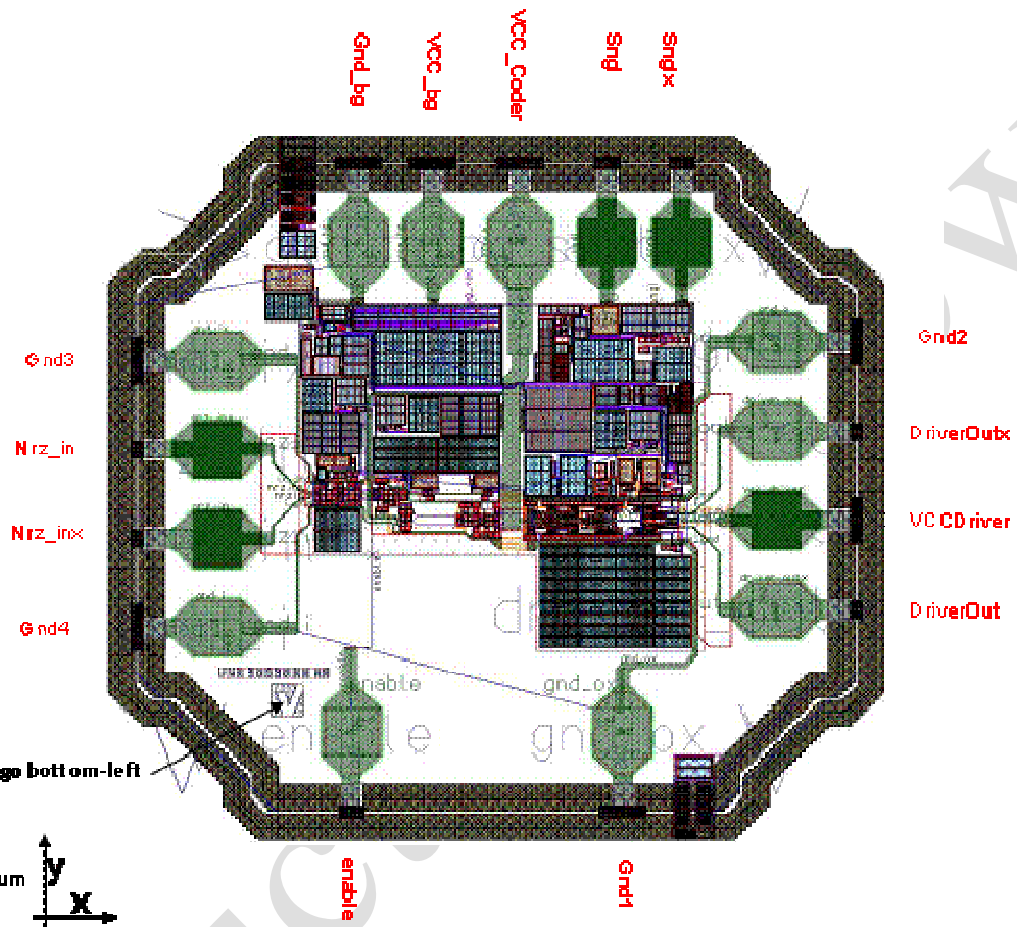
Main Features

- SiGe BiCMOS - Ft = 150GHz
- Data rate up to 25Gb/s
- 3 V / 480 mW typical bias @ 27°C
- Single or differential input / output
- Input amplitude: 300mV pp
- Output amplitude: 800mV pp diff (400mV on each 50Ω output)
- Temperature compensated
- ON and OFF state through an enable pin control

Functional Block Diagram



Chip pin out



« VectraWave » logo bottom-left

Name	Type	Description
enable	Digital input	Chip enable: switches the chip ON or OFF.
Gnd1*	Bias in/out	Ground for the driver output stage. To be used with Gnd2 as ground plane for coplanar access.
DriverOut	RF output	RF signal out. The driver uses a 50Ω resistor load in order to be consistent with 50Ω: has to be loaded if not used.
VCCDriver	Bias in/out	Positive bias for the driver output stage. The DC common output level to the output is directly dependent to this value.
DriverOut	RF output	RF signal out. The driver uses a 50Ω resistor load in order to be consistent with 50Ω: has to be loaded if not used.
Gnd2*	Bias in/out	Ground for the driver output stage. To be used with Gnd1 as ground plane for coplanar access.

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VWA 50030 AAAA DS Rev 0.11

VectraWave Proprietary information subject to change



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Snglx	Digital out	High (VCC) if no input signal
Sngl	Digital out	High if input signal: Snglx complementary
VCC_Coder	Bias in/out	Main chip bias: biases the chip drivers, the amplifier core and the first driver stages.
VCC_bg	Bias in/out	Chip reference voltage and current bias. Is separated from the main bias to ensure a proper DC filtering
Gnd_bg	Bias in/out	Chip reference voltage and current ground. Is not physically connected to the RF grounds.
Gnd3*	Bias in/out	Ground for input signal access. To be used with Gnd4 as ground plane for coplanar access.
Nrz_in	RF input	Digital signal input. DC is present on the access. Has to be DC decoupled from the external source by an external capacitor. Is 100Ω differential referenced to Nrz_inx.
Nrz_inx	RF input	Complementary digital signal input. DC is present on the access. Has to be DC decoupled from the external source by an external capacitor. Is 100Ω differential referenced to Nrz_in.
Gnd4*	Bias in/out	Ground for input signal access. To be used with Gnd3 as ground plane for coplanar access.

- All pads are octogonal (w / l μm²) = 66 / 105; except VCC_Coder = 75 / 105
- Die thickness = 0.28 mm (11 mils)
- No metallization on back side

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Electrical specifications

Electrical parameters	Conditions	Symbol	Min.	Typ.	Max.	Unit
<i>Chip bias</i>						
Supply voltage	VccCoder – VccBG	Vcc		3		V
	VccDriver		2.5	3	4	V
Current consumption OFF mode*	VccCoder; enable=0; T=27°C	VccCoder0		3		nA
	VccBG; enable=0; T=27°C	VccBG0	(100°C) 0.01	15	(-40°C) 28	uA
	VccDriver; enable=0; T=27°C	VccDriver0		27		pA
Current consumption ON mode*	VccCoder; enable=1	VccCoder1		90		mA
	VccBG; enable=1	VccBG1	(-40°C) 2		(100°C) 2.5	mA
	VccDriver; enable=1	VccDriver1		16		mA
<i>Data input (Nrz in and Nrz inx)</i>						
Input impedance	Single and differential modes	Zin		100		Ω
Amplitude range**	Single or differential input		2	300		mVpp
Frequency range***			0		40	GHz
<i>Driver Output</i>						
Output impedance	Single / Differential			50 / 100		Ω
Common mode voltage	Referred to VCCDriver			VCCDriver-0.350		V
Amplitude	Single			400		mVpp

* OFF → enable =“0”, ON → enable=“1”

** The Min value corresponds to the value which saturates the Driver output.

*** The frequency range is limited for low frequency, by the external decoupling capacitors.

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Absolute rating

Parameters	Conditions	Symbol	Min.	Typ.	Max.	Unit
Supply voltage	VccCoder – VccBG - VccDriver	Vcc	-0.5		4.6	V
Digital input	enable		-0.5		4.6	V
Storage temperature					TBC	°C

ESD protection

Parameters	Conditions	Symbol	Min.	Typ.	Max.	Unit
HBM* rating RF in/out	Clk, NRZin DriverOut				0.9	kV
HBM* rating analog	enable				2.3	kV
HBM* rating bias	VCC gnd				5.7	kV

*Human Body Model

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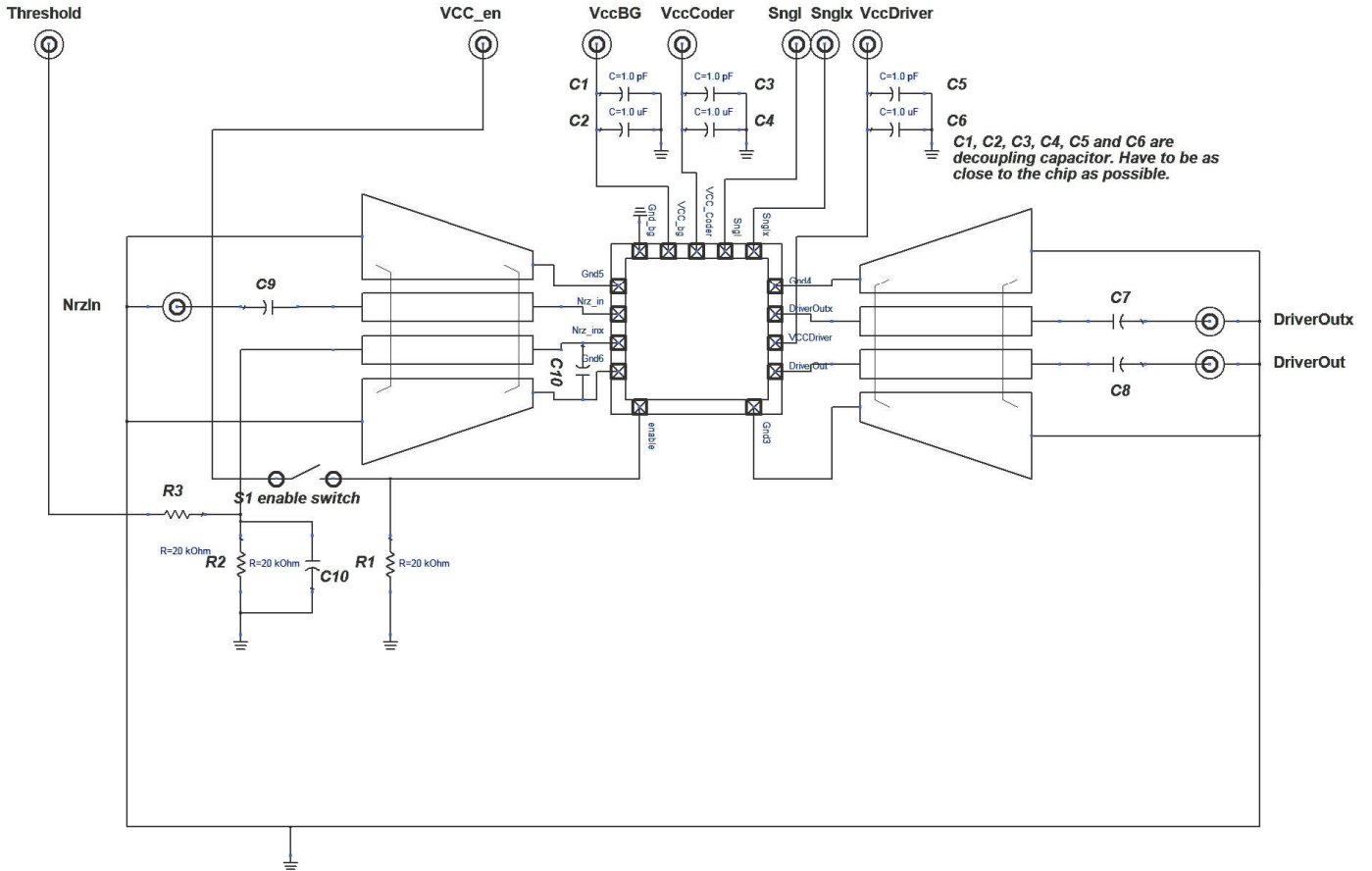


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Application schematic

Single IN, Differential OUT with cross point modification



Handling



These products are sensitive to electrostatic discharge and should not be handled except at a static free workstation. Take precautions to prevent ESD; use wrist straps, grounded work surfaces and recognized anti-static techniques when handling the IC.

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